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Design Of Data Acquisition System (DAS) With Lowpass Filter Based On Digital Signal Processing (DSP)

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ABSTRACT: *This Data Acquisition System (DAS) project is aimed at designing a "DAS with low pass filter based DSP". For the implementation of the design, 4 input channels were used; the amplitude of the input signal was 0 - +/- 500mV while the input signal frequency range was 0-5KHz. Furthermore, input impedance was > 10KOhms and the accuracy was <+/- 0.4% of 4 digits reading. Low pass filter must have cutoff of 1KHz (-3dB). The main element of DSP of family ADSP218x (Analog devices) was used. In addition, the power supply voltage was +5.5…. +7Volts and DAS was connected to PC through RS-232 interface. From our calculations, we found out that the additive and multiplicative errors are more than the value given in our task. We can decrease this value using compensation in the digital part of our system. Additive error can be decreased using subtraction of zero level code from every result of measurement, multiplicative error can be compensated by multiplying result of measurement by some coefficient, if the result is more than nominal value, we can compensate it using a coefficient that is less than 1, non – removable errors are non – linearity and resolution errors, the values added gives (0.061+0.0244) % = 0.085%. This value is less than it is given in the task, hence lies within the range of the error given in the task.*

KEYWORDS*- DAC, ADC, GPIB*

I. INTRODUCTION

DAS is the process of sampling signals that measure real world physical conditions and converting the resulting samples into digital numeric values that can be manipulated by a computer [10]. Data acquisition systems typically convert analog waveforms into digital values for processing. In the simplest way of description, An Engineer logging the temperature of an electrical plant on a piece of paper is performing data acquisition [7]. Based on the advancement of technology, this process has been simplified greatly, made more accurate and even more reliable through electronic equipment. This equipment can be a simple recorder all the way to being a more advance computer system. Data acquisition products work as a focal point in a system, bringing together a wide range of products such as sensors that indicate pressure flow, level, or temperature [9].

1.1 Main Elements and terms in DAS

- Digital to Analog Converter (DAC)
- Digital Input/Output (DIO)
- General Purpose Interface Bus (GPIB)
- RS 232
- RS 485
- Single ended input (SE)
- Aliasing
- Sample rate
- Oversampling
- Resolution
- Differential Input
- Analog to Digital Converter (ADC)

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1.2 Types of Data Acquisition Systems:

- Serial Communication Data Acquisition Systems
- USB Data Acquisition Systems
- Plug – in – board Data Acquisition Systems
- Parallel Port Data Acquisition Systems

1.3 Application of DAS

The applications of DAS can be organized into several parts:

Measurement:

When the process model is unknown, the quantities being measured may not be understood, thus measurement is the collecting of enough data to construct the unknown model [6].

Testing and Calibration:

This represents a situation where a device is being checked against its design standards of a certain parameters are made to establish the values of the other calibration parameters [6].

Control:

The system initiates a series of actions, measure them, and take the correct action if the desired results are not achieved [8].

2. TASK IMPLEMENTATION:

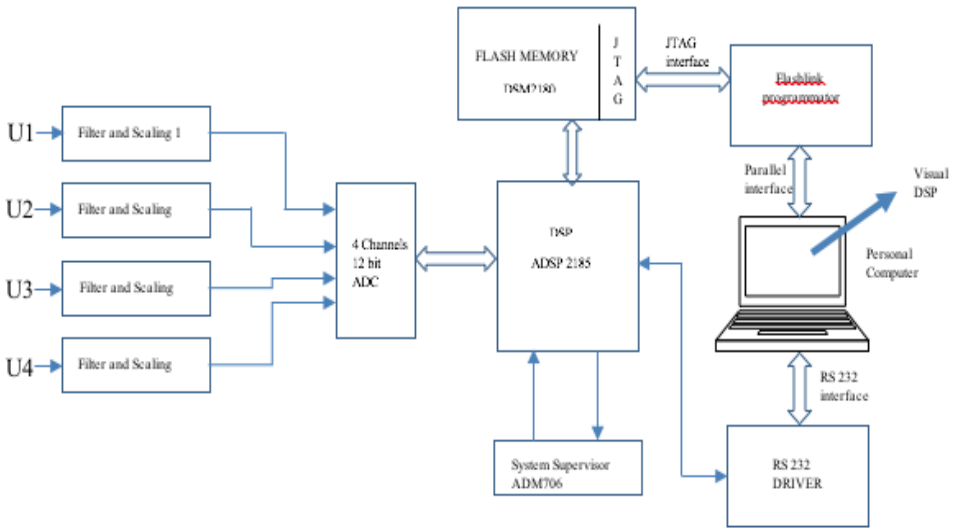


Fig. 1 Block diagram of the proposed Data Acquisition System

Description The main elements based on the task of DAS.

4 – Channels 12 bits ADC:

This is the block that takes the input signal after filtering and scaling block, it converts the analog signals to digital signal. The ADC block in this case will convert the analog input voltage to digital signal for processing [4].

DSP (ADSP-2185N):

This is the brain of the device, it is the block that keeps the registers, processors and memory, it carries out the major calculations and programming, in general all mathematical operations and units such as the MAC, ALU are here [9].

SYSTEM SUPERVISOR (ADM706):

System supervisor is responsible for monitoring the regulating power inputs and supplies. It also creates reset as shown in the figure above.

FLASH MEMORY (DSM2180) and JTAG:

DSM2180 is a system memory device used with popular digital signal processors from the Analog Devices [10]. DSM is referred to as digital signal processor system memory [11]. A DSM device brings In-System Programmable (ISP) flash memory, programmable logic, and additional I/O to digital signal processing system [11]. It provides flexibility of the flash memory and smart JTAG programming technique for both manufacturing and the field. It helps for the addition of large amounts of external flash memory to ADSP218x family for boot loading and for overlay memory [5]. JTAG in-system programming (ISP) reduces development time, simplifies manufacturing flow and lowers the cost of field upgrades. TAG interface eliminates the need for sockets and pre-programmed memory and logic devices [10].

RS-232:

This is one of the major methods of combining devices or instrument in DAS. They are used as interfaces for connection. It is one of the most commonly used serial communication interfaces. It is defined as the interface between data terminal equipment and data communication equipment using serial binary exchange [4].

FLASH LINK:

The data flash link is a 2.5 – 2.7 volts' serial interface flash memory ideally suitable for a wide variety of digital voice, image, program code and data storage. The serial interface facilitates hardware layout, increases system reliability, minimizes switching noise and reduces package size and active pin count. The device operates at clock frequencies up to 20mhz with typical active read current consumption of 4mA. All programming cycles are self-timed and no separate erase cycle is required before programming.

PERSONAL COMPUTER (PC):

Personal computer (PC) has become a very important tool in DAS, the pc serves as a plug-in point for other devices through interfaces for the evaluation of results. Programs are written in the computer to determine the functionality of our devices.

1. DETAILS DESIGN AND CALCULATIONS

3.1 DESIGN OF THE ANALOG CHANNEL OF DAS

This figure below (fig. 2) shows one analog input channel of DAS. The channel consists of scaling and shifting device, analog filter and ADC. Scaling and filtering device is used to scale input bipolar signal to the input of the filter, due to a single supply operation of all DAS devices we need a scale input signal to shift it to positive value. Scaling device has Kf coefficient of amplification for input bipolar signal.

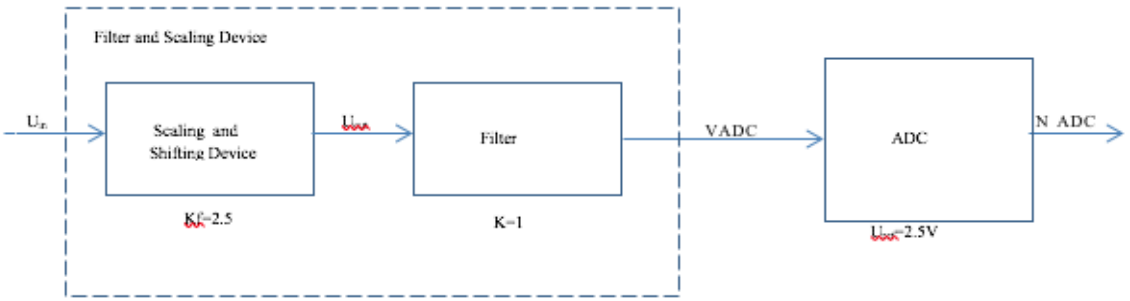


Fig. 2 Block diagram of one of the analog input channel.

II. METHODOLOGY

3.2 CALCULATION OF COEFFICIENT OF AMPLICATION (K_f)

Calculating K_f of our task parameters. According to the task, we have amplitude of input signal Uin = 500mV. If output signal of scaling device has amplitude Uout = 1.25V (for single power supply voltage Up= +3.3V), we can calculate K_f value as:

K_f = Uout / Uin = 1.25V / 0.5V = 2.5 (1)

3.3 CALCULATION OF SHIFT VOLTAGE (Uout_shift)

Calculating the shift level in the output of scaling device as

Uout_shift, Uout_shift = 0.5 * Vref,
where Vref is a reference voltage source for ADC. As will be shown later,
for ADC7294 Vref = 2.5V, so
Uout_shift = 0.5 * 2.5V = +1.25V. (2)

3.4 CALCULATION OF OFFSET VOLTAGE FOR SCALING AND SHIFTING DEVICE.

When calculating the offset voltage, we must have to know the coefficient of simplification for the input shift voltage. This value is 1+R2/R1.

As calculated earlier, the value = R2/R1 = 2.5 (3)
so coefficient of amplification for input shift voltage on the positive input of scaling device:
K_shift = 1+R2/R1=1+2.5=3.5 (4)
offset voltage = Uout_shift/K_shift,
hence offset voltage = 1.25V/3.5=0.3571V (5)
% offset voltage is approximately 0.3571V. (6)
A combination of the graph of the input voltage and the shift is shown below:

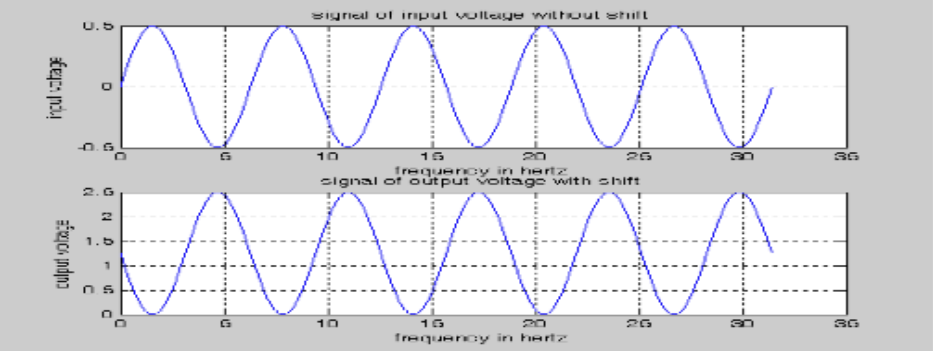


Fig. 3 scheme of input and output voltage

ANALOG INPUT ANTILIASING FILTER

Analog input filter is used as antialiasing type. According to the task, the given analog input bandwidth F_a; the requirements of the antialiasing filter are related not only to the sampling rate F_s but also to the desired system dynamic range. Dynamic range is the ratio of the largest expected signal which must be resolved in dB.

NYQUIST CRITERIA:

Using the Nyquist's criteria, we have that the sample frequency must or has to be greater than or equal to twice the cut-off frequency.
In other words F_s<2F_a (7)
Given: F_a = 5Khz,
then 2*5Khz is = 10Khz (8)
and by Nyquist's criteria F_s<2F_a, then F_s is ≥ 10Khz. (9)
Our analog to digital converter is a 12 – bit ADC and it has DR of 72dB. Since we have indicated that to get the most appropriate filter order, we have to get the sample rate to be ≥ 2x the cut – off frequency (F_s≥2F_a). To get a filter order, we use the relation according to the analog device application note.
M=DR / 6 * log2 (Fs/2Fa) (10)
Where M = filter order (dB)
DR = Dynamic Range
F_a = cut – off frequency
F_s = sample frequency
SLOPE: 6M dB / OCTAVE
We can obtain the right filter order if we use the cut – off frequency of not lower than 1Mhz. We have 4 channel 12 – bit ADC, hence, we divide the value of the cut – off frequency by 4.
So in this case we have:
1Mhz = 1000000hz/4 = 250000hz. (11)
M = DR/6*log2 (25) = M = 72/6*5 = 72/30 = 2.4 (12)
M = 2.4 (13)
Based on recommendations of our task, we can infer that any filter of order greater than 3 can work in this device. Hence; we use the filter of mode/order 5.

CALCULATION OF ANALOG INPUT ANTILIASING FILTER

To calculate the filter order there is need to know a lot of parameters used in the calculation. According to the task, K: Coefficient of filter (K=1)

Characters of this work has parameters such that there are four (4) input channels, that the amplitude of input signal must be between zero (0) to five hundred millivolts (500mV), that input signal frequency must be between zero (0) to five kilo hertz (5Khz), that input impedance must be greater or equal to 10 kilo ohms (10Kohms), that the accuracy of all my calculations must be less than ± 0.5% of reading +5 digits. Low pass digital filter must have cutoff frequency of one kilo hertz (1Khz) or minus 3 dB (-3dB), other characteristics are: that the main element must be DSP of the family ADSP218x (analog device), that the power supply voltage must be within the range of +5.5 to +7.0V, and that DAS must be connected to a PC through RS 232 interface.

ANALYSING THE CIRCUITRY STRUCTURE OF SCALING AND FILTERING DEVICE

If we know all parameters for scaling and shifting device, we can design electrical diagram.

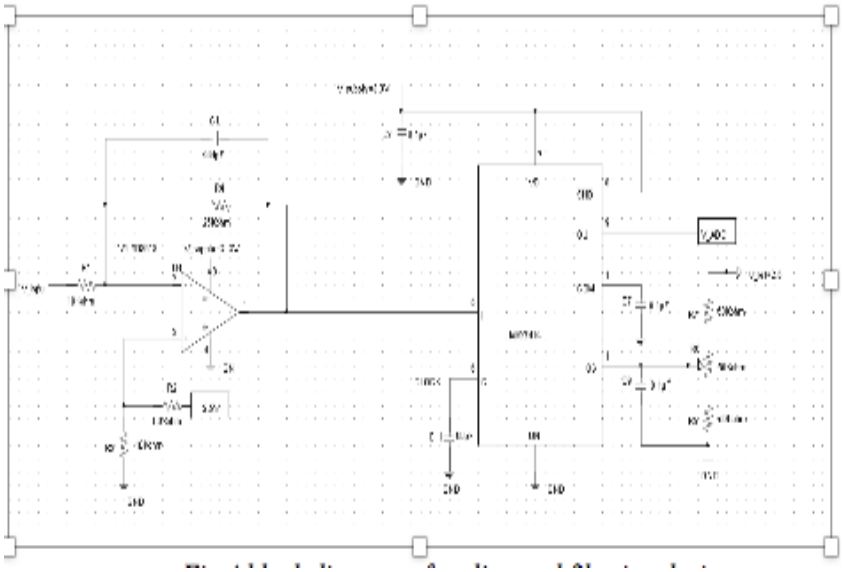


Fig.4 block diagram of scaling and filtering device

To analyze the circuitry structure of our device putting the shift voltage into consideration we have: the circuitry diagram showing the structure of the operational amplifier which is a single supply, rail to rail, low power FET – input operational amplifier. It belongs to the class of AD820. The operational amplifier is linked/connected to the filter which is a fifth – order, low pass, switched capacitor filter, it is a MAX7414 type filter.

5.1 CALCULATION OF RESISTANCES AND CAPACITANCES USING OFFSET AND REFERENCE VOLTAGES:

5.1.1 CALCULATION OF R1 and R2.

We know that our reference voltage (V_ref) = 2.5V

and our offset voltage (Vout_offset) = 0.0925V.

Hence; using the parameters of the non – inverting operational amplifier, we have that:

Uout_offset = Uout_shift / (1+R2/R1) (14)

0.3571V=1.25/(1+R2/R1),

supposing our R1=10Kohm,

1+R2/R1=1.25/0.3571

R2/R1=1.25/0.3571 – 1

R2 = 25Kohm.

5.1.2 CALCULATION OF R3 and R4:

From our analog device data shit, we have that the current that goes through R4 can be expressed as: I=V_ref/R3+R4 or

Uout_offset = I*R4 = V_ref*R4/R3+R4, (15)

taking the relation Uout_offset = V_ref*R4/R3+R4

we have; where Uout_offset = 0.3571V,

and V_ref=2.5V,

if R3 = 10Kohm

then R3/R4 = V_ref – Uout_offset/Uout_offset (16)

R4=Uout_offset*10Kohm/V_ref – Uout_offset (17)

R4=0.3571V*10Kohm/2.5V – 0.3571V = 3.571/2.143 = 1.66Kohm.

This cannot be found in the table of standard resistor values hence we take a rounded – up figure for our resistor as 1.6Kohm.

R4= 1.6Kohm.

5.1.3 CALCULATION OF CAPACITOR C1 OF THE SCALING AND FILTER DEVICE.

Z2=R2 ‖ (1/sC2) (18)

Vo(s)/Vi(s) = 1/Z1(s) Y2(s) (19)

Z1=R1 and Y2(s) = (1/R2) +sC2

to obtain Vo(s)/Vi(s) = -1/R

Z1=R1

Z2= ‖ R2 ‖ (1/sC2)

Vo(s)/Vi(s)=1/(R1/R2)+sC2R1 (20)

Assuming s=0, Vo/Vi = -R2/R1

Vo(s)/Vi(s)= (-R2/R1)/1+sC2R2

If s=jw k=R2/R1

K(jw) = (R2/R1)*1/1+jwC1R2

IK(jw)I=(R2/R1)*1/V1+wexp2(C1R2)exp2

Wo=1/C1R2 Wo=2π*fc where fc is the cut – off frequency

From the task, cut – off frequency = 5Khz

2π*fc =1/C1R2 C1=1/2π*fc*R (21)

We have to choose a Wo that is 3 times more than normal Wo, because we have to reduce error, if we choose a value that is equal to the value of the cut – off frequency of task, we would have error up to 40%, so we choose a higher value to reduce error up to 0.1% or 0.2%.

1/3*Wo*R2 = 1/25*103*6.28*5.10

C1=444pF

5.1.4 CALCULATE THE CLOCK SIGNAL (EXTERNAL AND INTERNAL CLOCK SIGNAL) of fig. 4

From the data sheet material for 5th order, low pass, switched – capacitor filters the external clock for MAX7414 family of SCFs is designed for use with external clocks that have a 50% ±10% duty cycle. Varying the rate of the external clock adjusts the corner frequency of the filter as follows:

Where:

F_c = cut – off frequency

F_clk = clock frequency

F-osc = oscillator frequency

C_osc = oscillator capacitor (capacitor of clock)

F_c = F_clk/100

When using internal oscillator, connect a capacitor (C_osc) between clk and ground. The value of the capacitor determines the oscillator frequency as follows:

F_osc (Khz) = 30*10exp3/C_osc (pF) (22)

It also states that we must minimize the stray capacitance at clk so that it does not affect the internal oscillator frequency. Vary the rate of the internal oscillator to adjust the filter's corner frequency by a 100:1 clock to corner ratio.

5.1.5 CALCULATION OF C_11 OF THE CLOCK CAPACITOR

To calculate the C_osc according to the data sheet in accordance with the cut – off frequency:

C_osc = 30*10exp3/F_osc=30*10exp3/F_c*100 (23)

=30*10exp3/5*100

=30000/500= 60pF (pico farad)

C_osc = 60pF

Hence, according to the diagram the value of the clock capacitance is 60pF.

5.2 REFERENCE INPUT VOLTAGE

The reference input voltage to the ADC as the reference output voltage of the 5th order real filter of the family of MAX7414 of the electrical scheme of scaling and filtering device, in this case as specified in the analog data sheet, the input reference input is 2.5V even as expressed in the task. The DC leakage current is ±1µA and input capacitance of 36Kohms. The test conditions from the analog data sheet specifies ±1 performance and a sample frequency of 1MSPS

ADC:

The AD7924 is a 12 – bit, high speed, low power, 4 channels, successive approximation ADCs. The parts operate within a nominal single voltage range of 2.7V to 5.25V power supply and feature throughout rates up to 1MSPS. The parts contain a low noise, wide bandwidth track/hold amplifier that can handle input frequencies in excess of 8Mhz. from the analog data sheet recommendation, the maximum power consumption is 2.7mA. from analog device data sheets, the ADC provides user with an on chip track and hold, A/D converter and a serial interface housed in a 16 lead TSSOP package. The AD7924 has a 4 single – ended channel sequencer, allowing the user to select a channel sequence through which the ADC can cycle with each consecutive CS falling edge. The ADC has an offset error of ±8% and a gain error of ±1.5%.

DSP (MICRO COMPUTER/MICRO CONTROLLER)

The ADC is connected to the DSP by a serial interface, the serial interface allows the part to be directly connected to a range of many different micro – processors. The serial interface in this case is TMS320C541 that uses a continuous serial clock and frame synchronization signals to synchronize the data transfer operation with devices like AD7924. The CS input allows easy interfacing between the TMS320C541 and the AD7924 without any glue logic required. The serial port is set up to operate in the burst mode with internal CLKX0. The control register data is loaded on the first 12 SCLK cycles.

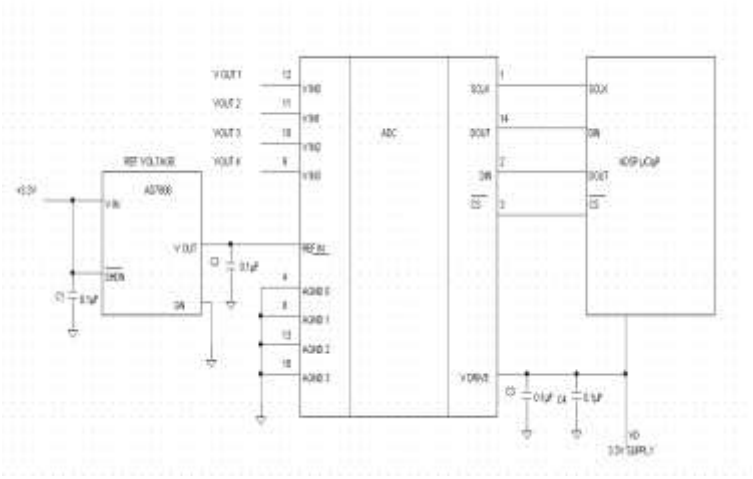


Fig. 5 Diagram of ADC with reference voltage source and DSP

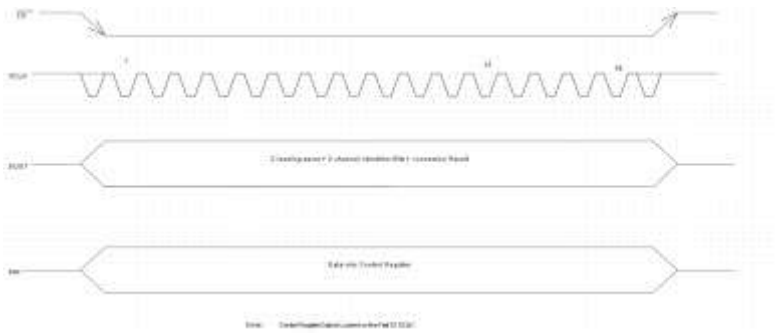


Fig. 6 Diagram of the normal operation mode of the clock diagram

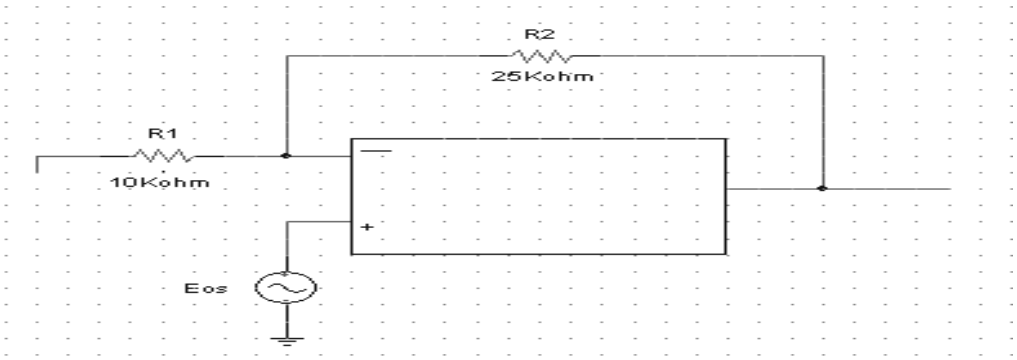
5. ANALYSIS OF ACCURACIES.

This chapter or section of the work analyzes the errors of the different devices that make up the DAS. Basically, what is in focus is the accuracies of the scaling device. In this regard, calculating the errors such as: additive error, multiplicative error. Furthermore, this chapter looks at errors of the filtering device, which will also be additive and multiplicative errors. Lastly, this chapter, discusses the errors of the ADC. This chapter is going to consider additive error, multiplicative error, on – linearity error and finally limited resolution error. The above-mentioned errors are not all the errors inherent in the system; however, the errors that will be analyzed can be considered the most critical errors of the system under consideration.

6.1 SCALING DEVICE

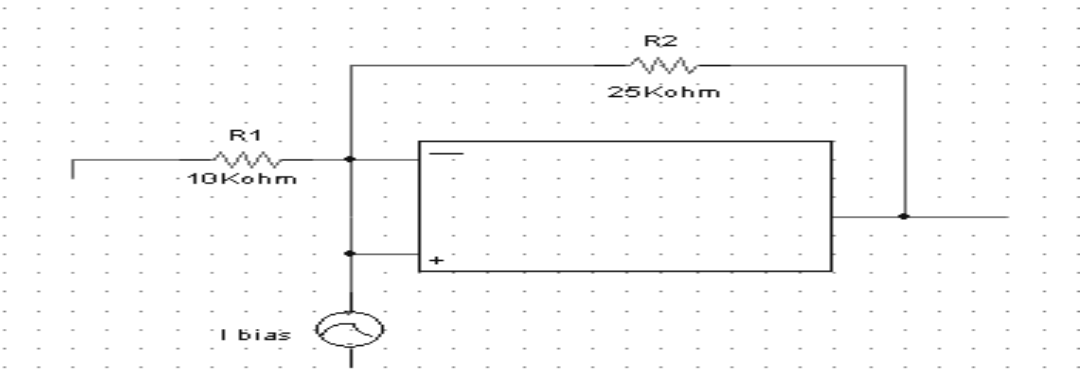
Additive Error:

As a first step, considering offset voltage and offset current is of significance. Our offset voltage is already known from analog device data sheet with maximum value as 65µV and our bias current is already known from analog device data sheet with maximum value of 1pA. To be able to know the additive error of the scaling device; we have to be able to ascertain the absolute errors of the offset voltage and bias current respectively.
To calculate the value of the absolute error of offset voltage and bias currents, it makes sense to look into the structure of the operational amplifier in consideration.



From analysis, we can conclude that the:

Absolute error for offset voltage: ΔV=Vos (1+(R2/R1)). (24)
From previous chapter, we have that R1 = 10KΩ; R2 = 25KΩ and Vos = 65µV (0.000065V), thus from the relation ΔV=Vos (1+(R2/R1)), we have: ΔV=0.00169V. Absolute Error of offset voltage: ΔV=0.00169V
Relative Error of offset voltage δV = (ΔV/Vnorminal)* 100% (25)
Absolute Error of Bias current: ΔVbias (26)



Absolute Error for Bias current: ΔVbias=Ibias*R2, (27)
again, we know from the previous chapters that R2=25KΩ and from analog device data sheets, we have that
Ibias=1pA= (28)
Thus, ΔVbias= 0.001*10-9*25000Ω= 0.25*10-7

ΔVbias= 0.25*10-7

Absolute Error of Bias current: ΔVbias= 0.25*10-7

Additive Error of offset voltage and Bias current

=ΔV+ΔVbias=0.00169V+0.25*10-7 =0.00169V (29)

Multiplicative Error:

The multiplicative error of the scaling device depends to a great extent on the values of the accuracies of the resistors, in this case R1 and R2.

To calculate this error, we have to take into consideration the absolute value of the coefficient of amplification K. IKI=R2/R1 and to find the relative of the absolute value of K IδKI

Generally, to find the absolute error of K: ΔK we have

ΔK=(δK/δRi)*ΔRi (30)

but K=R2/R1

ΔK :=(δ(K)/δR1)*ΔR1 + (δ(K)/δR2)*ΔR2 (31)

ΔK := (-R2/R12)*ΔR1 + (1/R1)*ΔR2

If we divide through by K and multiply through by 100% then we are directly calculating the relative multiplicative error. However from data sheets, we take our absolute error values of our resistors as 0.5%

(ΔK/K)*100%= - (ΔR1/1)*100% + (ΔR2/R2)*100% (32)

δK=δR1+δR2 ≤0.1%

6.2 FILTER DEVICE:

Additive Error:

For the filter device, the additive error is the same as the offset error from analog device data sheet additive error=25mV=0.025V

Multiplicative Error:

The electrical characteristics of the multiplicative error from analog device data sheet is given as ±0.2dB, from micro electric circuits we can calculate to get our error in relative form using the relation:

0.2dB=20log(ΔK/K) (33)

ΔK/K=100.2/20

But K=1 hence ΔK=100.2/20

K=100.2/20 =1.023

K-Kadc=1.023-1=0.023

δK=(ΔK/K)*100%=(0.023/1)*100%=2.3%

6.3 ADC:

This part will consider the errors of ADC. Additive; multiplicative error, we will look into ADC and reference; on – linearity error and limited resolution error.

Additive Error:

From analog device data sheet, we have that offset or additive error=±8, but this is expressed in code form to take the form which could be expressed in voltage, we have the relation below: it is necessary to consider the resolution. From analog device data sheet, we have that the resolution is equal to 12 in bits. To get it in normal form that can be used in the calculation we convert 12bits using: 212-1=4095

Additive error=Vref*8/4095 but we know from previous calculations that our reference voltage source= Vref=2.5V. additive error = 2.5*8/4095=0.00488V

Multiplicative Error:

The multiplicative error is divided into 2 parts:

1. Multiplicative error of ADC part
2. Multiplicative error due to reference source:

The multiplicative error of the ADC is as gain error according to analog data sheets and it is =±1.5, as usual for the conversion we have;

Vref*1.5/4095=2.5*1.5/4095=0.000916V= 0.000916/1.25*100%=0.073%

The multiplicative error due to reference source according to analog device data sheet is given directly as ±6=6mV=0.006V

0.006/1.25*100%=0.48%

Total multiplicative error for ADC = (0.48+0.073)=0.553%

Non – Linearity Error:

The non – linearity error has the differential and integral non – linearity errors.

Differential non – linearity error = -0.9/1.5
Integral non – linearity error=±1
Summation=2.5
Non – linearity error = Vref*2.5/4095=2.5*2.5/4095=0.001526V
0.001526/2.5*100%=0.061%
limited Resolution Error:
1/4095 x 100%/1=0.0244%
To get the complete error values,we have to sum all the various errors:
1. Additive error (ΔV additive) = (0.00169+0.025+0.00488)V =0.03157V
In % it would be 0.01357/2.5 x 100%=1.263%
2. Multiplicative error (ΔV multiplicative) = (0.1+2.3+0.553)%=2.953%
3.Non-Linearity error=0.061%
4. Limited Resolution error=0.0244%

From our calculations, we found out that the additive and multiplicative errors are more than the value given in our task. But we can decrease this value using compensation in the digital part of our system.
Additive error can be decreased using subtraction of zero level code from every result of measurement.
Multiplicative error can be compensated by multiplying result of measurement by some coefficient. If the result is more than nominal value, we can compensate it using a coefficient that is less than 1.
Non –Removable errors are Non-Linearity and Resolution errors. There values added gives (0.061+0.0244) %=0.085%.
This value is less that it is given in the task. Hence lies within the range of the error given in the task.

6. MATHLAB DESIGN FOR TESTING DSP FILTER

DSP filters can be design with the aid of computer application MATHLAB, there are many different types of filters available in the construction of filters using MATHLAB, in this case we will be using the Finite Impulse Response (FIR), A finite impulse response (FIR) filter is a type of a signal processing filter whose impulse response is of finite duration, because it settles to zero in finite time. The impulse response of an Nth-order discrete-time FIR filter lasts for N+1 samples, and then dies to zero. FIR filters can be discrete-time or continuous-time, and digital or analog.
Shown below is a simple MATHLAB program for our low pass filter considering our parameters in our task:

```
clc;
clear;
format long;
fs=10000;
fc=1000;
n=500;
Wn=fc/(0.5*fs);
b=fir1(n,Wn);
a=1;
fvtool(b,a);
```

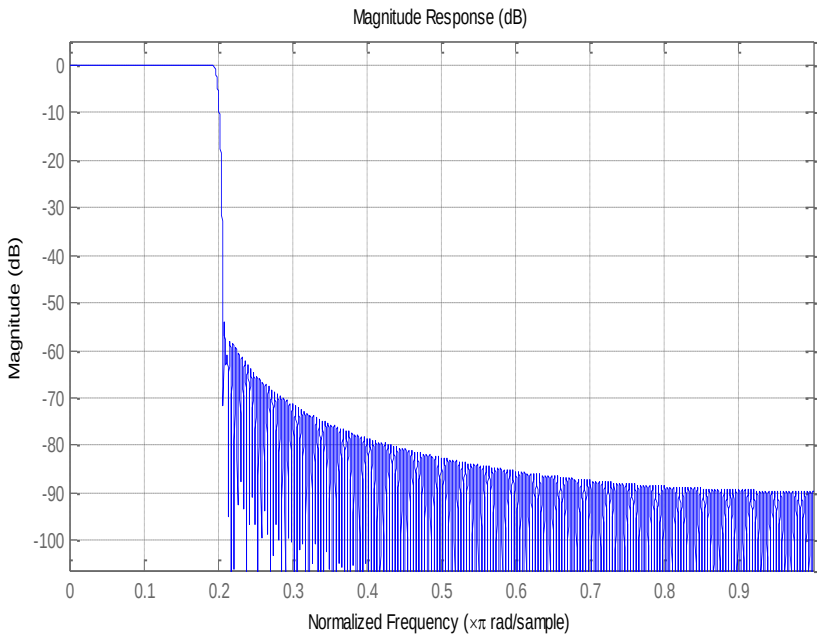


Fig. 6 Diagram of a design low pass filter with cutoff frequency = 1khz

III. CONCLUSION

Modern sampling and digital signal processing tools make it possible to replace analog filters with digital filters in applications that require flexibility and programmability. These applications include audio, telecommunications, geophysics and medical monitoring. You can use digital filters in MATHLAB to control parameters such as filter order, cutoff frequencies, amount of ripples, stopband ripples, and passband ripples. From our calculations, we found out that the additive and multiplicative errors are more than the value given in our task. We can decrease this value using compensation in the digital part of our system. Additive error can be decreased using subtraction of zero level code from every result of measurement, multiplicative error can be compensated by multiplying result of measurement by some coefficient, if the result is more than nominal value, we can compensate it using a coefficient that is less than 1, non – removable errors are non – linearity and resolution errors, the values added gives (0.061+0.0244) % = 0.085%. This value is less than it is given in the task, hence lies within the range of the error given in the task.

Digital filters have the following advantages over their analog counterparts:

- They are software programmable.
- They are stable and predictable.
- They do not drift with temperature or humidity and do not require precision components.
- They have a superior performance- to- cost ratio.

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