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Design of Data Acquizition System (DAS) With Rejective Digital Filter Based on Digital Signal Processing (DSP)

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Abstract: *This research was aimed at designing a "DAS with Rejective Digital Filter Based on DSP". The Design of the DAS based on DSP with the following characteristics:*
Number of inputs channels – 4; Amplitude of input signal 0±500 mV; Input signal frequency ranges: 0-5 kHz; Input impedance: >10 kOhms; Accuracy: <±0.4% of reading + 4 digits and Rejective digital filter must have central frequency: 50Hz and band ±2 Hz. There were other characteristics which included: Main element – DSP of family ADSP218x ("Analog Devices"), Power supply voltage: +5.5…+7 V, and DAS must be connected to PC through RS-232 interface. From our calculations, we found out that the additive and multiplicative errors are more than the value given in our task. But we can decrease this value using compensation in the digital part of our system.
Additive error can be decreased using subtraction of zero level code from every result of measurement.

I. INTRODUCTION TO DATA ACQUISITION SYSTEM

DAS is one of the first steps in analyzing data in digital signal processing. [5].

Before going ahead to discuss the entire project in detail, I think it would be of great importance to discuss or know what exactly DAS means. Moreso, it is necessary to know what hard or software to go alongside DAS for the parameters in question to function properly.

Data acquisition systems, as the name implies, are products and/or processes used to collect information to document or analyze some phenomenon [5]. In the simplest form, a technician logging the temperature of an oven on a piece of paper is performing data acquisition .As technology has progressed, this type of process has been simplified and made more accurate, versatile and reliable through electronic equiption.Equipment ranges from simple recorders,dataloggers to sophisticated computer systems .Data acquisition products serve as a focal point in a system; tying together ,a wide variety of products ,such as sensors that indicate temperature,flow,level or pressure. Some common data acquisition terms are shown below:

Analog-to-Digital Converter (ADC)
Digital-to Analog Converter (DAC)
Digital Input/Output (DIO)
Differential Input
General Purpose Interface Bus (GPIB)
Resolution
RS-232
RS-485
Sample Rate

 Received-12-07-2024, Accepted- 24-07-2024

Single-ended Input (SE)

1.2. TYPES OF DATA ACQUISITION SYSTEMS:

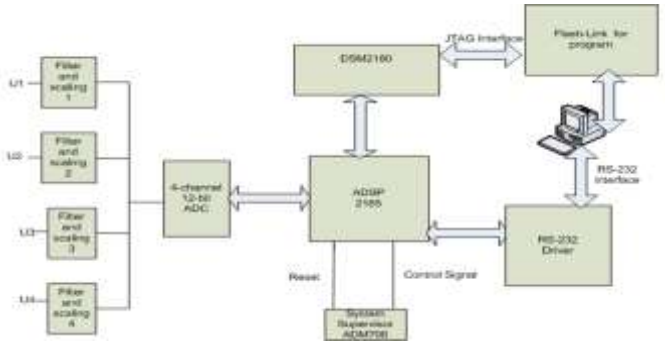
The following are the different types of DAS that are existent based on the distances it supports, the devices to be connected, the bandwidth size, the speed, the DAS Sample Rate, the power source, and as a matter of fact, the cost involved [1].

Serial Communication Data Acquisition System

USB Data Acquisition System

Data Acquisition Plug-In Boards

Parallel Port Data Acquisition System



Figs 1.1 DATA ACQUISITION SYSTEM BLOCK DIAGRAM

1.3 MAIN COMPONENTS OF DATA ACQUISITION SYSTEM

Taking the functions of each of the blocks we have:

1.3.1. The Analog filter and scaling block:

The filter and scaling block or unit is some sorts of signal conditioning circuitry which performs such functions as amplification, attenuation, and filtering. Filters have two major functions: 1-to separate signals that are combined with noise and 2-to restore signals that have been distorted in some way. These in other words mean to remove frequencies that are either above or below the sampling rate. In our case, the input analog filter must be a low pass filter type as shown below [1]:

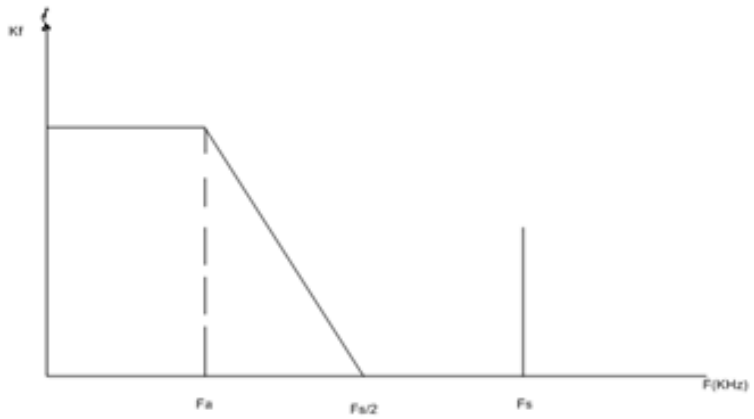


Fig 1.1

Basically, the signals are made to pass through the filters before it gets to the analog digital converter; in this case, the 4-channel 12 bit ADC.

1.3.2. The 4-channel 12 bit ADC block:

This block is the block that takes the input signal after filtering and scaling block. It is the block that converts the analog signals to its digital form. In this case, the ADC is going to convert the analog input voltage to some digital signal for further processing.

1.3.3. The ADSP2185:

This is the main brain of the device. It is in this block that the registers, processors and memory are kept. This block carries out major calculations and programming. In general all mathematical operations and units such as the ALU, MAC etc, are in this block.

1.3.4. The system supervisor ADM706:

The ADM block is a block that is responsible for monitoring the regulating the power inputs and supplies. It also creates reset as shown in the diagram.

1.3.5. The DSM2180 and JTAG:

The DSM2185 is a system memory device for use with digital signal processing from the popular analog devices. DSM means digital signal processor system memory. A DSM device brings In-system programmable (ISP) flash memory, programmable logic, and additional I/O to DSP system. It provides flexibility of the flash memory and smart JTAG programming technique for both manufacturing and the field. It helps for the addition of large amounts of external flash memory to ADSP218x family for boot loading and for overlay memory. TAG In-system programming (ISP) reduces development time, simplifies manufacturing flow and lowers the cost of field upgrades. TAG interface eliminates the need for sockets and pre-programmed memory and logic devices.

1.3.6. RS-232 DRIVER:

The RS-232 is one of the main methods of combining devices or instrument in Data Acquisition System (DAS). So basically; they are used as interfaces for connection. It is one of the most common serial communication interfaces. It is defined as the interface between data terminal equipment and data communication equipment using serial binary data exchange.

1.3.7. The Flash-Link for program:

The data flash-Link is a 2.5 to 2.7volts serial interface flash memory ideally suitable for a wide variety of digital voice, image, and program code and data storage. The simple serial interface facilitates hardware layout, increases system reliability, minimizes switching noise and reduces package size and active pin count.

The device operates at clock frequencies up to 20MHz with typical active read current consumption of 4mA.All programming cycles are self-timed and no separate erase cycle is required before programming.

1.3.8. The PC:

The PC has become a very important tool in the Data Acquisition System. The computer serves as a plug-in point for the other devices through interfaces for the evaluation of results. Moreso, programs are written in the computers to determine the functioning of our devices.

II. LITERATURE REVIEW

2.1. DETAIL DESIGN OF THE ANALOG CHANNEL OF DAS.

PART 1.

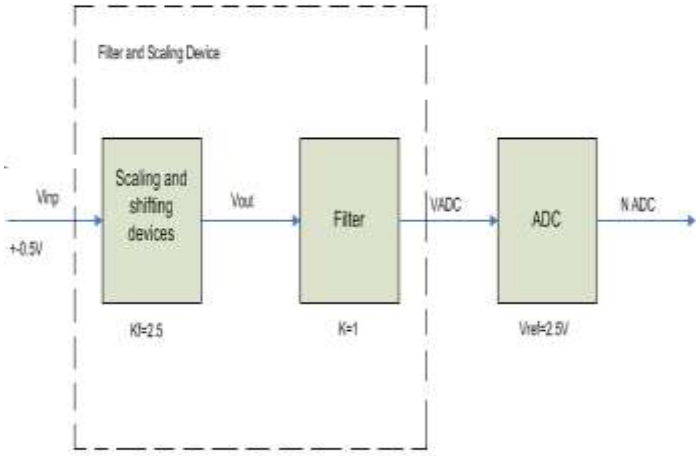


Fig.2.1 Block-diagram of the one analog input channel

On the Fig.2.1 is shown block-diagram of one analog input channel of DAS. The channel consists of Scaling and Shifting devices, analog filter and ADC.
Scaling and Shifting device is used to scale input bipolar signal to the input of filter [2]. Due to a single supply operation of all DAS devices we need a scale input signal so as to shift it to a positive value.
Scaling device has K_f-coefficient of amplification for input bipolar signal.

CALCULATION OF COFFICIENT OF AMPLIFICATION (k_f)

Let's calculate K_f for our task's parameters. According to the task [1], we have amplitude of input signal Uinp=100 mV. If output signal of scaling device has amplitude Uout=1.25V (for single power supply voltage Up=+3.3V), we can calculate K_f value as:

K_f=Vout/Vinp=1.25V/0.5V=2.5V (1.0)

2.3. CALCULATION OF SHIFT VOLTAGE (Vout_shift)

Let's calculate shift level in the output of scaling device as Vout_shift, Vout_shift = 0.5*Vref, (1.1)
Where Vref is a reference Voltage source for ADC. As will be shown later, for ADC AD7294 Vref = 2.5V, so

Vout_shift = 0.5*2.5V=+1.25V. (1.2)

Analog input filter is used as antialiasing type. According to [1], the given analog input bandwidth f_a; the requirements of the antialiasing filter are related not only to the sampling rate F_s but also to the desired system dynamic range. Dynamic range is the ratio of the largest expected signal which must be resolved in dB [1].

2.4. CALCULATION OF THE FILTER ORDER

For us to be able to calculate the filter order there is need to know a lot of parameters used in the calculation. According to [1], before we can go on, we need to acquaint ourselves with the following:
K_f: coefficient of amplification
K: Coefficient of Filter (k=1)
DR: Dynamic Range
M: Filter Order (dB)

SLOPE=6M dB/OCTAVE
From [2], I am given the following parameters:
That there are 4 input channels.
That the amplitude of input signal must lie between 0 to 500mV
That the input signal frequency must also lie between 0 to 5 KHz
That the input impedance must be greater or equal to 10Kohms
That the accuracy of all my calculations must be < ±0.4% of reading +4 digits.
That the rejective digital filter must have central frequency of 50 Hz and Band ±2Hz.
Other characteristics include:
That our main element must be DSP of the family ADSP218x (analog device)
That the power supply voltage must lie within the range of +5.5 to +7.0V
That the DAS must be connected to a PC through RS-232 interface.

2.5. NYQUIST CRITERIA:

Using the Nyquist's Criteria, we have that the Sample Frequency must or has to be greater or equal to twice the cut-off Frequency [3].
That is to say:
$F_s<2F_a.$ (1.3)
Given:
$F_a=5$ KHz.

Then,
$F_s\geq10$ KHz
Our analog to digital converter is a 12-bit ADC and it has DR of 72dB according to [1].
Since we have said that to get the most appropriate filter order, we have to have the sample rate ≥2x the cut-off frequency ($f_s\geq2f_a$).
To get a filter order, we use the relation according to the "analog device application note"

$M=DR/6*\log (Fs/2Fa)$ (1.4)

Where M=filter order
DR=Dynamic Range
F_a:cut-off frequency
F_s: sample frequency

We can obtain the right filter order if we use the cut-off frequency of not lower than 1MHz [3].
But we have 4-channel 12-bit ADC, hence, we divide the value of the cut-off frequency by 4.So in this case we have:

1MHz=1000000HZ/4 = 250000 Hz.

$M=72/6*\log2 (250000/10000)$ (1.5)
$M=72/6*\log2 (25)$ %log2 (25) =4.6439; approximately 5%

M =72/6*5=72/30=2.4
M=2.4. (1.6)
Based on the recommendations of [1], we can infer that any filter of order greater than say 3 can work in this device. Hence; we use the filter of mode/order 5.

2.6. CALCULATION OF OFFSET VOLTAGE FOR SCALING AND SHIFTING DEVICE.

From the diagram of the SCALING AND SCALING DEVICE we have that to calculate the offset VOLTAGE WE MUST KNOW COEFFICIENT OF SMPLIFICATION FOR INPUT SHIFT

VOLTAGE.THIS VALUE IS: 1+R2/R1. (1.7)

As calculated earlier, the value = R2/R1=2.5

So coefficient of amplification for input shift voltage on the positive input of scaling device:

K_shift=1+R2/R1=1+2.5=3.5 (1.8)

Offset voltage=Vout_shift/K_shift

Hence Offset Voltage=1.25V/3.5=0.3571V %offset voltage approximately 0.3571V%

A combination of the graph of the input voltage and the shift is shown below:

2.7. DIAGRAM OF INPUT/OUTPUT VOLTAGE

The plot:

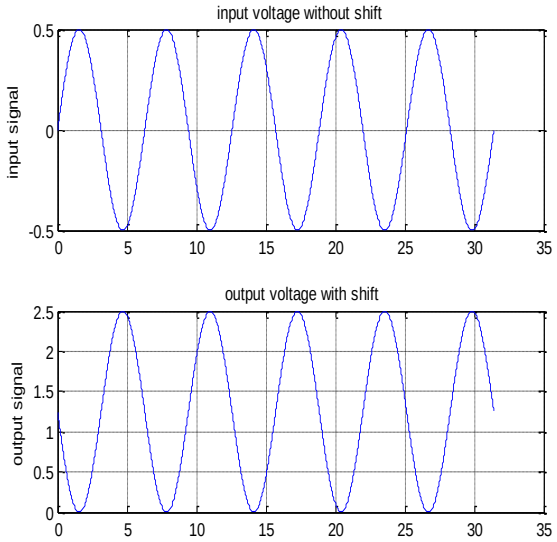


Fig 2.2. DIAGRAM OF INPUT AND OUTPUT VOLTAGE

To analyze the circuitry structure of our device putting the shift voltage into consideration we have:

This circuitry diagram showing the structure of the Operational Amplifier which is a single supply, Rail to Rail, Low Power FET-Input OP Amp. It belongs to the class AD820.

The Operational Amplifier is linked/connected to the filter which is a fifth-order, Low pass, Switched Capacitor Filter. It is a MAX7414 type filter.

If we know all parameters for Scaling and Shifting Device we can design electrical scheme, see fig.2.3

2.8. CALCULATION OF RESISTANCES AND CAPACITANCES USING THE OFFSET AND REFERENCE VOLTAGES:

2.8.1. CALCULATION OF R1 and R2.

From [1], we know that our reference voltage (V_ref) =2.5V and our offset voltage (Vout_offset) =0.3571V.

Hence using the parameters of the non-inverting operational Amplifier, we have that:

Vout_offset=Vout_shift/ (1+R2/R1) (1.9)

0.3571V=1.25/ (1+R2/R1)

Supposing our R1=10Kohm
1+R2/R1=1.25/0.3571
R2/R1=1.25/0.3571-1

R2=25kohm.

2.8.2. CALCULATION OF R3 and R4

From the fig 2.3 and from our analog devices data shit, we have that the current that goes through R4, I can be expressed as:

I=V_ref/R3+R4 or (2.0)
Vout_offset=I.R4=V_ref.R4/R3+R4
Taking the relation Vout_offset=V_ref.R4/R3+R4 we have;
Where Vout_offset=0.3571V, and V_ref=2.5V
If R3=10Kohm then
R3/R4=V_ref-Vout_offset/Vout_offset
R4=Vout_offset.10Kohm/V_ref-Vout_offset
R4=0.3571V.10Kohm/2.5V-0.3571V=3.571/2.143=1.66Kohm.
This can not be found in the table of standard resistor values hence we take a rounded-up figure for our resistor as 1.6Kohm.
R4=1.6Kohm.

2.8.3. CALCULATION OF CAPACITOR C1 OF THE SCALING AND FILTER DEVICE.

Z2=R2|| (1/sC2) (2.1)
Vo(s)/Vi(s) =1/Z1(s) Y2(s) (2.2)
Z1=R1 and Y2(s) = (1/R2) +sC2 to obtain (2.3)
Vo(s)/Vi(s) =-1/R (2.4)

From our task, cut-off frequency is 5 KHz.

$$C1 := \frac{1}{2\pi \cdot fc \cdot R2} \qquad (2.5)$$

$$2\pi \cdot f_c = \blacksquare \cdot \frac{1}{C1R2}$$

$$\frac{1}{3 \cdot Wo \cdot R2} = \blacksquare \cdot \frac{1}{25 \cdot 10^3 \cdot 6.28 \cdot 5 \cdot 10^3 \cdot 3}$$

If we know all parameters for Scaling and Shifting Device we can design electrical scheme, as seen below.

2.8.4. ELECTRICAL SCHEME OF SCALING AND FILTERING DEVICE

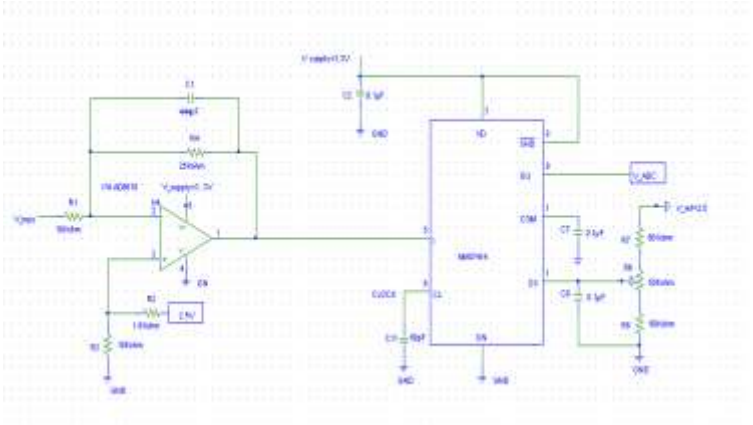


Fig 2.3. electrical scheme of scaling and filtering device.

2.8.5. How to calculate the clock signal (external and internal clock clock signal) of Fig 2.3?

From the data sheet material got from the internet for 5th order, low pass, switched-capacitor Filters the external clock for MAX7414 family of SCFs is designed for use with external clocks that have a 50% +- 10% duty cycle[3]. Varying the rate of the external clock adjusts the corner frequency of the filter as follows:
Where:
F_c=cut-off frequency
F_clk=clock frequency
F_osc=oscillator frequency
C_osc=the oscillator capacitor (capacitor of clock)

F_c=F_clk/100 $C1 := 444pF$ **(2.6)**

When using internal oscillator, connect a capacitor (C_osc) between clk and ground. The value of the capacitor determines the oscillator frequency as follows:

F_osc(KHz)=30X10exp3/C_osc(pF) (2.7)

It also states that we must minimize the stray capacitance at clk so that it does not affect the internal oscillator frequency. Vary the rate of the internal oscillator to adjust the filter's corner frequency by a 100:1 clock-to-corner ratio.

2.8.6. To Calculate C_11 of the clock capacitor

To calculate the C_osc according to the data sheet in accordance with the cut-off frequency:

S_osc=30X10exp3/F_osc (2.7)
=30X10exp3/F_c.100=30x10exp3/5.100
=30000/500=60pF (Pico Farad)
S_0sc=60pF.

Hence, according to the diagram fig 5 the value of the clock capacitance is 60pF.

2.8.7. The Reference Voltage:
The reference input voltage to the ADC as the reference output voltage of the 5th order real filter of the family of MAX7414 of the electrical scheme of scaling and filtering device (fig 2.3). In this case, as specified in the

analog data sheet, the input reference input is 2.5V even as expressed in the task. The DC leakage current is ±1µA max and input capacitance of 36KΩ.The test conditions from the analog data sheet specifies ±1 performance and a sample frequency of 1MSPS [3].

The ADC.

The AD7924 is a 12-bit, high speed, low power, 4-channel, successive –approximation ADCs.The parts operate within a nominal single voltage range of 2.7V to 5.25V power supply and feature throughout rates up to 1 MSPS[4].The parts contain a low noise, wide bandwidth track/hold amplifier that can handle input frequencies in excess of 8MHZ.From the analog data sheet recommendation, the maximum power consumption is 2.7mA.From analog device data sheets ,the ADC provides user with an on-chip track and hold, A/D converter and a serial interface housed in a 16-lead TSSOP package[8]. The AD7924 has a four single-ended channel sequencer, allowing the user to select a channel sequence through which the ADC can cycle with each consecutive CS falling edge. The ADC has an offset error of ±8% and a gain error of ±1.5% [9].

The DSP (Microcomputer/Microcontroller)

The DSP is connected to the ADC by a serial interface. The serial interface allows the part to be directly connected to a range of many different microprocessors. The serial interface, in this case a TMS320C541, uses a continuous serial clock and frame synchronization signals to synchronize the data transfer operation with devices like the AD7924.The CS input allows easy interfacing between the TMS320C541 and the AD7924 without any glue logic required. The serial port is set up to operate in burst mode with internal CLKX0[7].

2.8.8. SCHEME OF ADC WITH REFERENCE VOLTAGE SOURCE AND DSP

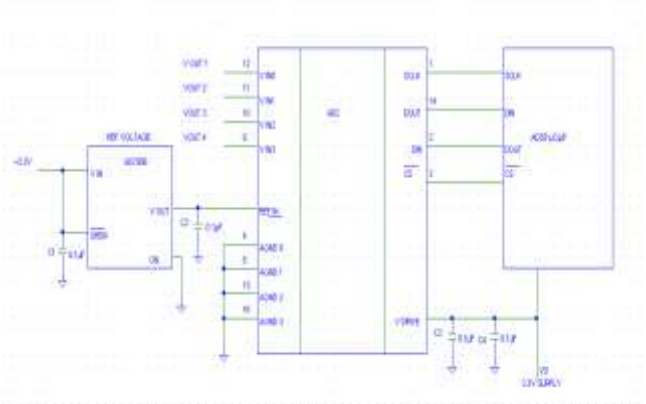


FIG 2.4. SCHEME OF NORMAL OPERATION MODE OF THE CLOCK DIAGRAM.

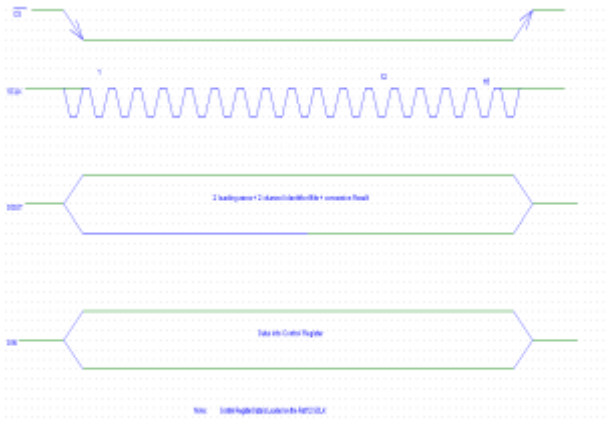


Fig 2. The control register data is loaded on the first 12 SCLK cycle

III. RESULTS

3.1ANALYSIS OF ACCURACIES

In this chapter, I would be analyzing the errors of the different devices that make up the Data Acquisition System. So basically, we would be looking into the accuracies of the Scaling device. In this regard, we would be calculating the errors such as: Additive error and Multiplicative error. In addition, this chapter would also look into errors of the Filtering device, which would also be additive and multiplicative errors. Lastly; this chapter would discuss the errors of the ADC.Under the ADC,this chapter is going to consider additive error, multiplicative error, non-linearity error and finally limited resolution error. The afore-mentioned errors are not all the errors existent in the system; all the same, the errors that are going to be discussed or analyzed could be considered the major errors of the system under consideration.

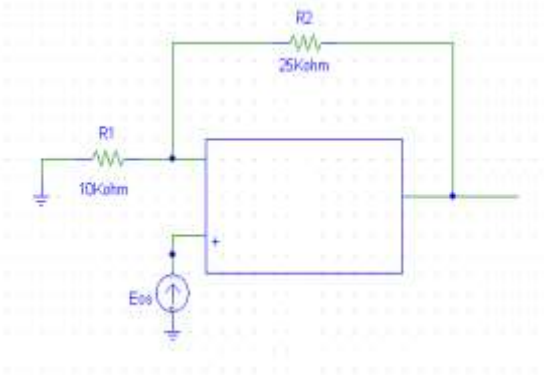
3.1.1. SCALING DEVICE:

3.1.1. a. Additive error:

For the additive error, we have to consider offset voltage and offset current first. Our offset voltage is already known from analog device data sheet with maximum value as Vos=65µV and our Bias current is already known from analog device data sheet with maximum value I bias=1pA [1]. But to be able to know the additive error of the Scaling device; we have to be able to ascertain the absolute errors of the offset voltage and bias current respectively.

To calculate the value of the absolute error of offset voltage and bias currents, it makes sense to look into the structure of the operational amplifier in consideration.

1. Absolute Error of offset Voltage: ΔV



From analysis, we can conclude that the:

Absolute error for Offset voltage: ΔV=Vos (1+R2/R1) (2.8)

From the previous chapter, we have that R1=10K Ω, R2=25K Ω and Vos=65µV (0.000065V)

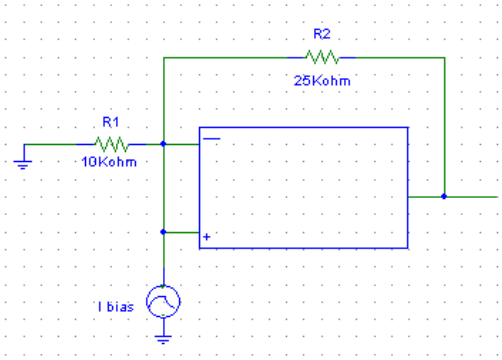
Thus, from the relation ΔV=Vos (1+R2/R1), we have:

ΔV=0.00169V=1.69mV

Absolute Error of offset Voltage: ΔV=0.00169V

Relative Error of offset Voltage (∂V) = (ΔV/Vnominal) x100%=

2. Absolute Error of Bias Current: ΔVI bias



Absolute Error for Bias current: ΔI=IbiasxR2

Again, we know from the previous chapter that R2=25K Ω and from analog device data sheets, we have that I bias=1pA=0.00000000000001A=1x10exp-11mA.

Thus, ΔI=0.00000000001Ax25000 Ω =0.000000025V

ΔVI bias=0.000000025V=2.5x10exp-5mV.

Absolute Error of Bias Current: ΔVI bias=0.000000025V=2.5x10exp-5mV

Additive Error of offset Voltage and Bias Current =ΔV+ΔVIbias=0.00169V+0.000000025V=0.00169V=1.69mV

3.1.1. b. Multiplicative Error:

The multiplicative error of the scaling device depends to a great extend on the values of the accuracies of the resistors. In this case, R1 and R2 [8].

To calculate this error, we have to take into consideration the absolute value of the coefficient of amplification K [8].

|K|=R2/R1 and to find the relative of the absolute value of K |**∂K|**

Generally, to find the absolute error of K: **Δ**K we have:

ΔK= (∂K/**∂**Ri) x **Δ**Ri but K=R2/R1 (2.9)

$$\Delta K := \frac{\delta(K)}{\delta R1}\cdot\Delta R1 + \frac{\delta(K)}{\delta R2}\cdot\Delta R2 \qquad (3.0)$$

$$\Delta K := \frac{-R2}{R1^2}\cdot\Delta R1 + \frac{1}{R1}\cdot\Delta R2 \qquad (3.1)$$

If we divide through by K and multiply through by 100% then we are directly calculating the relative multiplicative error. However, from data sheets, we take our absolute error values of our resistors as 0.05% [1].

(ΔK/K) x100%=- (**Δ**R1/R1) x100%+ (**Δ**R2/R2) x100% (3.2)

∂k=∂R1+∂R2 ≤ 0.1%

3.1.2. FILTER DEVICE:

3.1.2. a. Additive Error:

For the filter device, the additive error is the same as the offset error from analog device data sheet

Additive error=25 mV

3.1.2. b. Multiplicative Error:

The electrical characteristics of the multiplicative error form analog device data sheet is given as **±0.2dB.**

From micro electric circuits by Sedra/Smith we can calculate to get our error in relative form using the relation [9]:

0.2dB=20log (**Δ**K/K) (3.3)

$$\frac{\Delta K}{K} = 10^{\frac{0.2}{20}} \quad (3.4)$$

But K=1. Hence **Δ**k=10^0.2/20

$$k = 10^{\frac{0.2}{20}} = 1.023$$

K-kadc=1.023-1=0.023

∂K=Δk/K x 100%=0.023/1 x 100%=2.3%

3.1.3. ADC:

This part of chapter 3 would consider the errors of the ADC. These errors are:
Additive; multiplicative-under multiplicative error, we would be looking into ADC and Reference; on-linearity error and lastly Limited Resolution error.

3.1.3. a. Additive Error:

From analog device data sheet, we have that offset or additive error =±8
But this is expressed in code form to take to the form which could be expressed in Voltage, we have the relation below:
Below we go into the calculation, it is necessary to consider the resolution.
From analog device data sheets we have that the resolution is equal 12 in bits. To get it in normal form that can be used in the calculation we convert 12 bits using:

$$2^{12} - 1 = 4095 \quad (3.5)$$

Additive Error=Vref x 8/4095 But we know from previous calculations that our reference Voltage source: Vref=2.5Volts.
Additive Error= 2.5 X8/4095=0.00488Volts**= 4.88mV**

3.1.3. **b. Multiplicative error**

The multiplicative error is divided into two parts: 1. Multiplicative error of the ADC part and 2. The multiplicative error due to reference source.

1. The Multiplicative error of the ADC is same as gain error according to analog device data sheets and it is =±1.5
As usual for the conversion we have; Vref x 1.5/4095=2.5 x 1.5/4095=0.000916V=**0.916mV**
0.000916/1.25 x 100%=0.073%
2. The Multiplicative error due to reference source according to analog device data sheet is given directly as ±6=6mV=0.006V=**6mV**
0.006/1.25 x 100%=0.48%
Total multiplicative error for ADC= (0.48+0.073) =0.553%

3.1.3. c. Non-Linearity Error:

For the Non-Linearity Error we have the differential and integral non-linearity errors.
Differential Non-linearity Error =-0.9/1.5
Integral Non-Linearity Error=±1

Summation=2.5
Non-Linearity Error=Vref x 2.5/4095=2.5 x 2.5/4095=0.001526V=**1.526mV**
0.001526/2.5 x 100%=0.061%

3.1.3. d. limited Resolution Error:
1/4095 x 100%/1=0.0244%
To get the complete error values, we have to sum all the various errors:

3.1.4. SUMMATION of ALL ERROR TYPES

1. Additive error (ΔV additive) = (0.00169+0.025+0.00488) V =0.03157V=**31.57mV**
In % it would be 0.01357/2.5 x 100%= 1.263%
2. Multiplicative error (ΔV multiplicative) = (0.1+2.3+0.553) %=2.953%
3. Non-Linearity error=0.061%
4. Limited Resolution error=0.0244%

From our calculations, we found out that the additive and multiplicative errors are more than the value given in our task. But we can decrease this value using compensation in the digital part of our system.
Additive error can be decreased using subtraction of zero level code from every result of measurement.
Multiplicative error can be compensated by multiplying result of measurement by some coefficient. If the result is more than nominal value, we can compensate it using a coefficient that is less than 1.
Non –Removable errors are Non-Linearity and Resolution errors. There values added gives (0.061+0.0244) %=0.085%.
This value is less that it is given in the task. Hence lies within the range of the error given in the task.

IV. DISCUSSION

4.1. Design of Rejective Digital Filter based on Digital Signal Processing.
We suppose that in our input signal there are some power noise. In the task, we have that the power noise has a frequency of 50Hz and a small band of ±2Hz.Our noise sources could be from electrical mains, cables and other instruments that supply power source to our electrical/electronic devices.
The purpose of our task is to eliminate these noises using digital signal processing.
For the design of our filter we must know the Sample frequency, Power Noise central Frequency, Power Noise Frequency Range and the Filter Type which is Rejective Filter in our case.
The design proper has to do with ascertaining the filter coefficient and study the behaviour of the designed filter. This filter can be designed using MATLAB tool box.

From filter design reference guide in the design toolbox help we have that:
IirnotchSecond-order IIR notch filter
Syntax
[num,den] = iirnotch (W_0, bw)
[num,den] = iirnotch (W_o, bw, ab)
Description [num, den] = iirnotch (w0, bw) turns a digital notching filter with the notch located at W_o, and with the bandwidth at the -3 dB point set to bw. To design the filter, W_o must meet the condition 0.0 W_o 1.0, where 1.0 corresponds to pi radians per sample in the frequency range. The quality factor (Q factor) q for the filter is related to the filter bandwidth by q W_o/bw, where W_o is the frequency to remove from the signal. [Num, den] = iirnotch (W_o, bw, ab) returns a digital notching filter whose bandwidth, bw, is specified at a level of -ab decibels. Including the optional input argument ab lets you specify the magnitude response bandwidth at a level that is not the default -3 dB point such as -6 dB or 0 dB.
From my task, it is given that:
The frequency bandwidth=±2Hz.

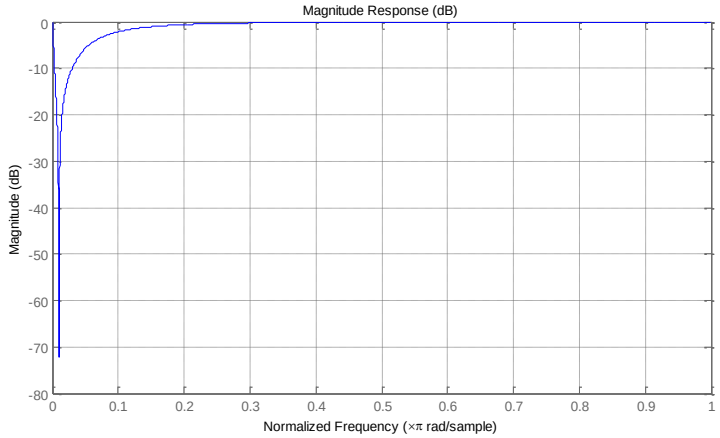
The frequency range (fo), given=50Hz
Our sample frequency (fs), according to task=10 KHz = 10000 Hz.

4.1.1. Matlab, the program using all given parameters is:

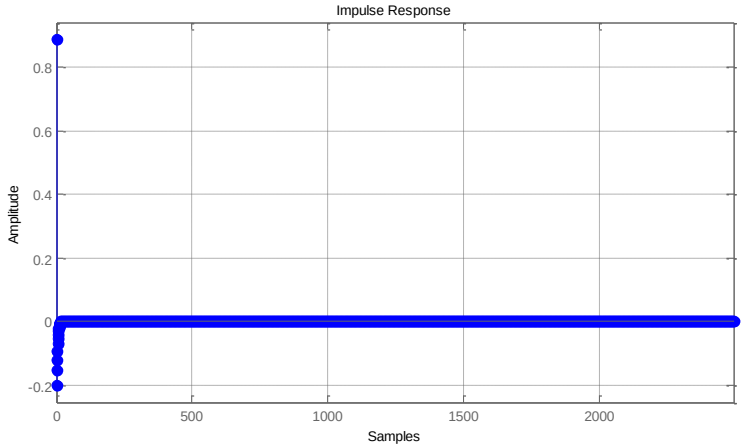
```
Clear;
clc;
fo=50;
df=2*2;      % this is the bandwidth from task%
Wo = 50/ (10000/2);
bw=df/50
Q=wo/bw;
[b, a] = iirnotch (Wo, bw);
fvtool (b, a);
```

4.1.2. Different Responses:

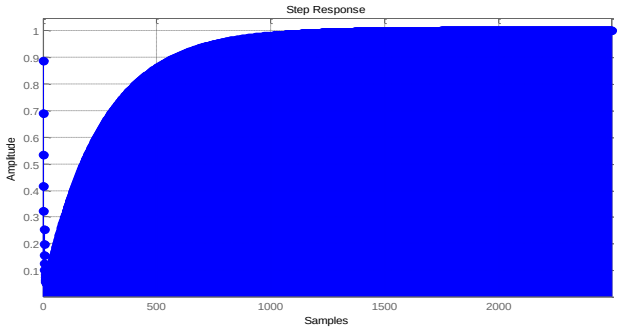
4.1.2. a. Full View of Magnitude Response:



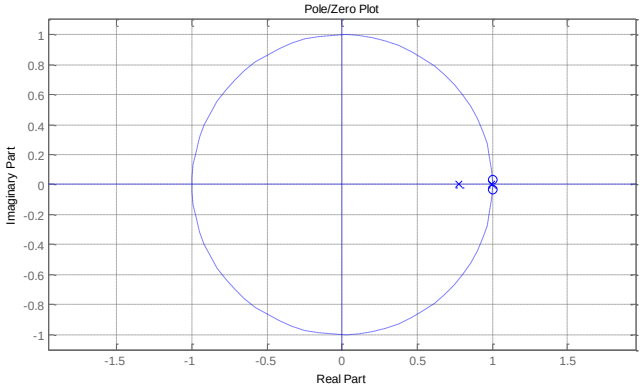
4.1.2.b. The impulse response diagram is:



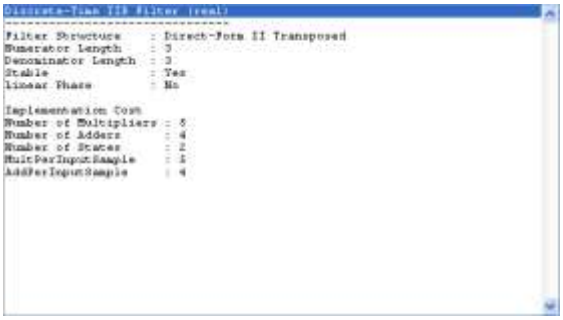
4.1.2.c. The step response diagram is:



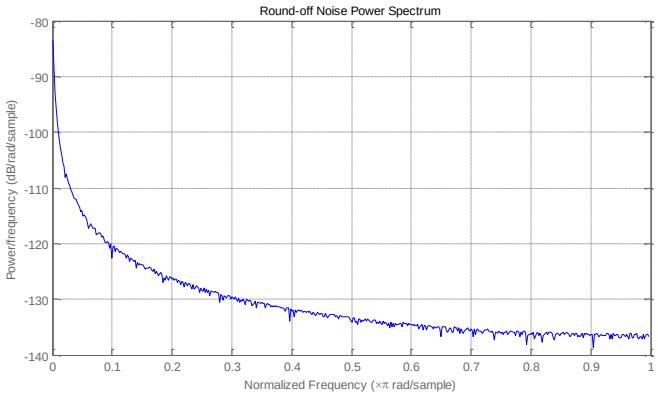
4.1.2. d. The pole/zero plots are:



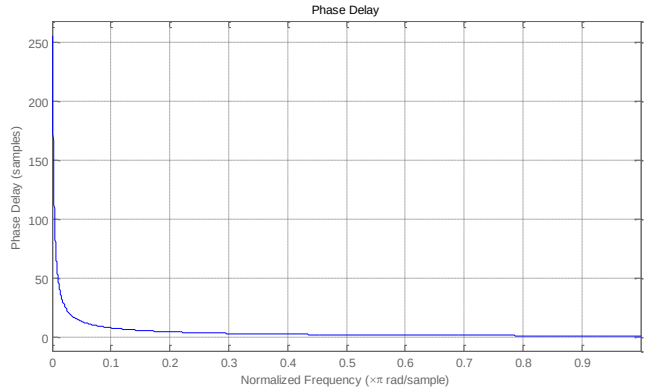
4.1.2. e. Table of parameters:



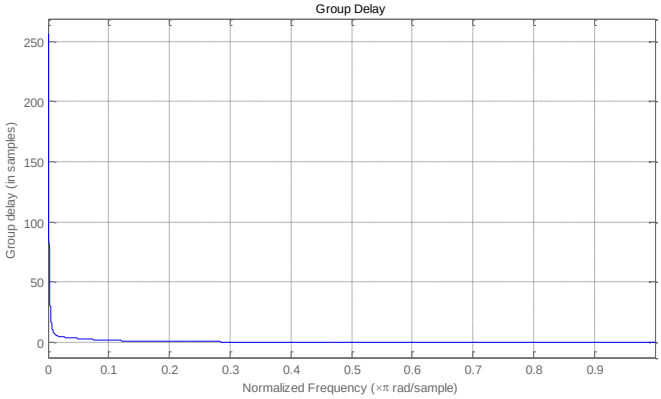
4.1.2. f. Round off Noise power spectrum:



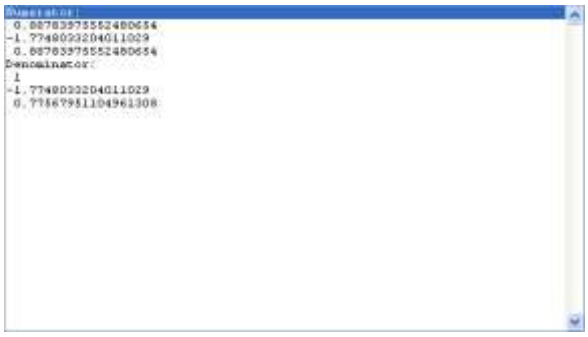
4.1.2. g. Phase Delay:



4.1.2. h. Group Delay:



4.1.2. i. The coefficients [a, b], are shown



To get the appropriate filter coefficients, we have to divide the values by the modular maximum value of coefficients.

Choosing maximum value as 1.7748033204011029

The first values for numerators are [b values]:

B [1] =0.500246841618572, B [2] = -1, B [3] =0.500246841618572

The values for denominators after division by the maximum coefficient for denominators [a] are:

A [1] = 0.563442714189875, A [2] = -1, A [3] = 0.437050969047269

After this is done, the filter coefficients must be rounded-up as follows to be able for simulation use.

For numerators we have [b]:

B [1] =0.50024, B [2]-1, B [3] 0.500244

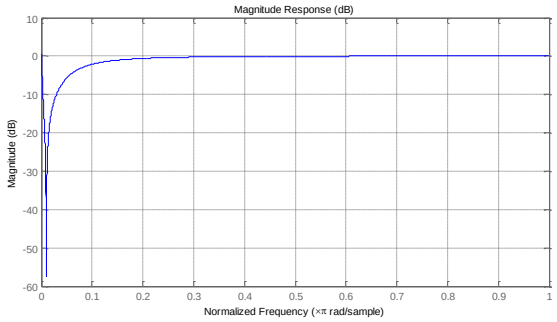
for the denominators, we have [a]:

A [1] =0.563416, A [2] =-1, A [3] =0.437042

4.2. The program of the full view of the magnitude response with the rounded filter coefficients is:

```
Clear;
clc;
fo=50;
df=2*2;      % this is the bandwidth from task%
wo = 50/(10000/2);
bw=df/50;
Q=wo/bw;
[b,a] = iirnotch(wo,bw);
Figure (1);
fvtool(b,a);
b= [0.500244 -1 0.500244];
a= [0.563416 -1 0.437042];
fvtool(b,a);
```

4.2.1. The figure of the full view of the magnitude response with rounded coefficients is:



All this, shows, our plot and filter is correct or within the required limits.

4.2 PRACTICAL IMPLEMENT OF FILTER FUNCTIONS USING DSP.

Compared to the FIR filter, an IIR filter can often be much more efficient in terms of attaining certain performance characteristics with a given filter order. This is because the IIR filter incorporates feedback and is capable of realizing both poles and zeroes of a system transfer function, whereas the FIR filter is only capable of realizing the zeroes (although the FIR filter is still more desirable in many applications, because of the features such as stability and the ability to realize exactly linear phase response [4].

4.21. Direct form of IIR filter

The IIR filter can realize both the poles and zeroes of a system because it has a rational transfer function, described by polynomials in z in both numerator and the denominator [2].

$$H(z) = \frac{\sum_{k=0}^{M} \left(b_k \cdot z^{-k}\right)}{1 - \sum_{k=1}^{N} \left(a_k \cdot z^{-k}\right)} \qquad (3.6)$$

The difference equation for such a system is described by the following:

$$y(n) = \sum_{k=0}^{M} b_k \cdot x(n-k) + \sum_{k=1}^{N} a_k \cdot y(n-k) \qquad (3.7)$$

In most applications, the order of the two polynomials M and N are the same.

The roots of the denominator determine the pole locations of the filter, and the roots of the numerator determine the zero locations. There are, of course, several means of implementing the above transfer function with an IIR filter structure .The "direct form" structure.

Note that there is a single delay line buffer for the recursive and non-recursive portions of the filter (Oppenhei and Schafer's Direct Form 11).The sum-of-products of the a values and the delay line values are first computed ,followed by the sum-of-products of the b values and the delay line values.

4.2.2. PROGRAM FOR DIGITAL FILTER

```
 Module diriir_sub;
{
  Direct From 11 IIR Filter Subroutine
  Calling parameters
        MR1=Input sample (x[n])
        MR0=0
         I0->Delay line buffer current location (x [n-1])
         L0=Filter length
         I5-> Feedback coefficients (a [1], a [2], a [3])
         L5=Filter length – 1
         I6->Feed forward coefficients (b [0], b [1], b [2])

         L6=Filter length
         M0=0
         M1, M4=1
         CNTR=Filter length -2
         AX0=Filter length -1

Return Value
  MR1=output sample (y[n])
  I0->delay line current location (x [n-1])
  I5->feedback coefficients
  I6->feed forward coefficients
```

```
Altered Registers
   MR0, MY0, MR

Computation Time
     (N-2) + (N-1) +10 + 4 cycles (N=M=filter order)
All coefficients and data values are assumed to be in 1.15 formats

}

.Entry diriir;

Diriir:  MX0=DM (I0, M1), MY0=PM (15, M4);
         D0 pole loop UNTIL CE;
Pole loop: MR=MR+MX0 *MY0 (SS), MX0=DM (I0, M1), MY0=PM (I5, M4);
          MR=MR+MX0 * MY0 (RND);
          CNTR=AX0;
          DM (I0, M0) =MR1;
          MR=0, MX0=DM (I0, M1), MY0=PM (I6, M4);
          DO zero loop UNTIL CE;
Zero loop: MR=MR+MX0 * MY0 (SS), MX0=DM (I0, M1), MY0=PM (I6, M4);
           MR=MR+MX0 *MY0 (RND);
           MODIFY (I0, M2);
           RTS;
```

4.2.3. Conclusion

The plot of the responses using the parameters given in the task and the response of the one with rounded up coefficients are exactly the same. Hence we can affirm that our task of filter responses is correct.

We design the filter which removes some noise using Matlab.In any case, it should be noted that since IIRNOTCH gives only the filter coefficients, we need to round up these coefficients realized in this chapter and use a standard program to realize the real IIR digital Filter; as shown in section 5.3.

Our system is designed as a DAS with Rejective Digital Filter Based on DSP, taking into account all the given factors in the task. All the elements of the Data Acquisition System were carefully chosen in accordance with the requirements of the task-the DSP, ADC etc

All errors related to both input/output devices have been calculated. From our calculations, we found out that the additive and multiplicative errors are more than the value given in our task. But we can decrease this value using compensation in the digital part of our system.

Additive error can be decreased using subtraction of zero level code from every result of measurement.

Multiplicative error can be compensated by multiplying result of measurement by some coefficient. If the result is more than nominal value, we can compensate it using a coefficient that is less than 1.

Non –Removable errors are Non-Linearity and Resolution errors. There values added gives (0.061+0.0244) %=0.085%.

This value is less that it is given in the task. Hence lies within the range of the error given in the task.

As clearly evidient, our Data Acquisition System is ready and according to the primary requirements and theoretical calculations, it is successful and if implement practically would perform both efficiently and effectively.

V. References

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